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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,800	11/08/2001	Mark A. Gerber	SC11588TK	7112

23125 7590 10/24/2002

MOTOROLA INC
AUSTIN INTELLECTUAL PROPERTY
LAW SECTION
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EXAMINER	
ROMAN, ANGEL	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 10/24/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/008,800	Applicant(s) GERBER ET AL.	
	Examiner Angel Roman	Art Unit 2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 August 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *16-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of Group I, claims 1-15 in Paper No. 4 is acknowledged. The traversal is on the ground(s) that the examiner failed to show that the process as claimed could be used to make a materially different product. This is not found persuasive because the product as claimed can also be made by another and materially different process, e.g., a resin compound could be used instead of the tape.

The requirement is still deemed proper and is therefore made FINAL.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Hosoya U.S. Patent 5,795,799 A.

Hosoya discloses a method for forming a package device, comprising; providing a package substrate having a first surface along, a first plane and providing a second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane (see figure 3A); placing a first integrated circuit 4 in the cavity (see figure 3B); placing a second integrated circuit 4' adjacent to the first integrated circuit 4 outside the cavity (see figure 3F); and depositing encapsulating material 6 over the first integrated circuit 4 and the second integrated circuit 4' (see figures 3C and 3F). The step of depositing comprises; depositing a first portion of the encapsulating material 6 over the first integrated circuit 4 prior to the step of placing the second integrated circuit 4' (see figure 3C); and depositing a second portion 6' of the encapsulating material over the second integrated circuit 4' (see figure 3F). Hosoya also discloses placing a third integrated circuit 7' adjacent to the second integrated circuit 4' prior to the step of depositing a second portion of encapsulating material (see figure 4). The integrated circuits have, first pads 3 on the first side and second pads 3'

on the second side; the first integrated circuit is place on the first side and the second integrated circuit is placed on the second side; electrical connections are formed between the first integrated circuit and the first pads and the second integrated circuit and the second pads (see figure 3F). The first integrated circuit 4 is placed on the first side prior to the second integrated circuit 4' being placed on the second side (see figure 3B). The first integrated circuit is electrically connected by wires 5 to the first pads prior to the second integrated circuit being electrically connected to the second pads (see figure 3B).

5. Claims 3-7 and 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Seki et al. U.S. Patent 6,022,759.

Seki et al. discloses a method of forming a package device, comprising; providing a package substrate having a first side and a second side and having first pads on the first side and second pads on the second side (see figure 15); placing a first integrated circuit 152 on the first side (see figure 20) and a second integrated circuit 151 on a second side; electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads (see figure 22); and testing the first integrated circuit and the second integrated circuit by applying, test probes to the first pads and the second pads (see column 16, lines 15-25). The step of attaching is further characterized by the first integrated circuit being placed on the first side prior to the second integrated circuit being placed on the second side. The first integrated circuit is electrically connected to the first pads prior to the second integrated circuit being

electrically connected to the second pads. The package substrate has a cavity between the first plane and the second plane (see figure 22). The encapsulating material is deposited over the first integrated circuit and the second integrated circuit by depositing a first portion of the encapsulating material over the first integrated circuit prior to the step of placing the second integrated circuit; and thereafter depositing a second portion of the encapsulating material over the second integrated circuit (see figure 22). The package substrate further comprises first pads on the first surface, second pads on the second surface, first bond fingers on the first surface, and second bond fingers on the second surface, further comprising; electrically connecting by wire bonding the first integrated circuit to the first pads; electrically connecting the second integrated circuit to the second pads (see figure 22). The package substrate further comprises an electrically conductive supporting member 126 along, the second plane of the substrate between the first integrated circuit and the second integrated circuit (see figure 20).

6. Claims 3-5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Lin et al. U.S. Patent 5,239,198.

Lin et al. discloses a method of forming a package device comprising; providing a package substrate 12 having a first side and a second side and having first pads 14 on the first side and second pads 16 on the second side; placing a first integrated circuit 20 on the first side and a second integrated circuit 27 on a second side (see figure 3); electrically connecting the first integrated circuit to the first pads and the second integrated circuit to the second pads (see figure 3); and testing the first integrated circuit

and the second integrated circuit by applying, test probes to the first pads and the second pads (see column 4, lines 30-34). The step of attaching is further characterized by the first integrated circuit being placed on the first side prior to the second integrated circuit being placed on the second side (see figures 1-3). The step of electrically connecting is further characterized by the first integrated circuit being electrically connected to the first pads prior to the second integrated circuit being electrically connected to the second pads (see figures 1-3).

7. Claims 1, 6, 7, 11, 14 and 15 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura U.S. Patent 6,333,566 B1.

Nakamura discloses a method for forming, a package device, comprising: providing a package substrate 2 having, a first surface along a first plane and second surface along a second plane, wherein the package substrate has a cavity between the first plane and the second plane (see figure 2a); attaching a tape 8 to the package substrate 2 along the first plane (see figure 2(a)); placing a first integrated circuit 1 on the tape and in the cavity (see figure 2(a); depositing encapsulating material over the first integrated circuit (see figure 2(c)); removing the tape (see figure 2(e)); placing a second integrated circuit adjacent to the first integrated circuit outside the cavity; and depositing encapsulating material over the second integrated circuit (see figure 7). The package substrate further comprises a tape-supporting member 8 along, the second plane of the substrate and a step of removing, the supporting member prior to step of placing the second integrated circuit (see figure 2(d)). The package substrate further comprises first pads on the first

surface and second pads on the second surface and first bond fingers on the first surface and second bond fingers on the second surface, further comprising; electrically connecting the first integrated circuit to the first pads; electrically connecting, the second integrated circuit to the second pads (see Abstract).

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

10. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura U.S. Patent 6,333,566 B1 in view of Higgins, III U.S. Patent 5,291,062.

Nakamura is applied as above but lacks anticipation on testing, the first integrated circuit and the second integrated circuit by applying, test probes to the first pads and the second pads. Higgins, III discloses testing an integrated circuit by applying test probes (see column 4, lines 32-40). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit in the primary reference of Nakamura by applying probes as disclosed in Higgins, III, since unnecessary packaging cost may be prevented by testing the circuit functionality.

11. Claims 3-5, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hosoya U.S. Patent 5,795,799 A in view of Higgins, III U.S. Patent 5,291,062.

Hosoya is applied as above but lacks anticipation on testing the first integrated circuit and the second integrated circuit by applying test probes to the first pads and the second pads. Higgins, III discloses testing an integrated circuit by applying test probes (see column 4, lines 32-40). In view of this disclosure, it would have been obvious to a person having ordinary skills in the art at the time the invention was made to test the integrated circuit in the primary reference of Hosoya et al. by applying probes as disclosed in Higgins, III, since unnecessary packaging cost may be prevented by testing the circuit functionality.

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Lin et al., Ugon, Brown, Kumai et al., Chen, Akram et al., Akram, Farquhar et al., Fee et al., Mine et al., Bernardoni et al. and Rathmell et al. disclose methods for packaging semiconductor devices providing package substrates comprising plural devices.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angel Roman whose telephone number is (703) 306-0207. The examiner can normally be reached on Monday-Friday 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7724 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

AR
October 20, 2002

John F. Niebling
Supervisory Patent Examiner
Technology Center 2800